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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,536	08/27/2001	Jeong Kwon Lee	P-199	2797

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EXAMINER	
PRIETO, BEATRIZ	
ART UNIT	**PAPER NUMBER**
2142	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,536	LEE, JEONG KWON	
	Examiner	Art Unit	
	Prieto Beatriz	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Amendment filed 03/14/05, claims 1-2, 8-9, 16 and 19-20 have been amended, and claims 28-31 have been added. Claims 1-31 remain pending.

2. Amendments to claims 8, 9 and 16, obviated rejection under 112, second paragraph, rejection is thereby, withdrawn.

3. Amendments to the specification obviated objection noted in previous office action, thereby objection is withdrawn.

Claim Rejections - 35 USC § 102

4. Quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action may be found in previous office action.

5. Claims 1-4, 6, 8-11, 13-17, 19-23, 26, and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Shetty (US 5,791,014).

Regarding claim 1, Shetty discloses an apparatus comprising:

a connector configured to provide a connection port to a data circuit terminating equipment (fig. 2A, item 116; col. 3, lines 23-25);

a multi-protocol transceiver coupled to the connector and configured to transmit and receive a plurality of protocol signals through the connector (fig. 2A, item 220A);

a CPU having a serial communication control function coupled to the multi-protocol transceiver to process data according to a communication environment of a connection network (fig. 2A, item 140), said data received from or for transmission to a communication network coupling one or more peripherals (column 27, lines 5-25, column 10, lines 65-column 11, line 29); and

a programmable logic device (PLD) coupled to sense a change in a connection state of the connector through a prescribed control line and to transfer the sensed information to the CPU (fig. 2A, items 202 and 110; col. 17, lines 66-67 - col. 18, line 1; col. 18, lines 26-32).

Regarding claim 2, Shetty discloses that the prescribed control line comprises an interrupt request (IRQ) signal line (col. 6, line 21), an acknowledgement (ACK) signal line (col. 17, line 17), a chip select (CS)

signal line (col. 6, line 26), a protocol mode line (col. 13, lines 51-54), and a cable state sensing line (col. 17, lines 39-41).

Regarding claim 3, Shetty discloses that the IRQ signal line, the ACK signal line, and the CS signal line are coupled between the PLD and the CPU (fig. 2A, item 146; col. 5, lines 65-67 - col. 6, lines 1-7) and that the protocol mode line and the cable state sensing line are coupled between the PLD and the connector (fig. 2A, item 110).

Regarding claim 4, Shetty discloses that the IRQ signal line and the ACK signal line comprise a control line (fig. 2A, item 146) to carry information to the CPU indicating a change in the connection state of the connector, wherein the state is one of connection and disconnection (col. 17, lines 39-41, col. 6, lines 20-23, col. 17, lines 50-52).

Regarding claim 6, Shetty discloses that the PLD uses a pull-up resistor to determine a hardware protocol (col. 13, lines 51-54).

Regarding claim 8, Shetty discloses a method comprising:

sensing a change in a connection state of a connector (fig. 2A, item 116) between a router (fig. 2A, item 101) and a data circuit terminating equipment (DTE) (fig. 2A, item 122; col. 17, lines 39-41);

carrying sensing information to a CPU when change in the connection state of the connector is sensed (col. 17, lines 39-41, col. 6 lines 20-23 and col. 17 lines 50-52);

initializing parts of the router and normalizing communication environments based on the sensing information (col. 8, lines 54-58).

Regarding claim 9, Shetty discloses that sensing the change in the connection state of the connector comprises sensing a change of a connected or disconnected state of the connector (col. 17, line 41).

Regarding claim 10, Shetty discloses that the connected state is determined by a low logic state of a prescribed connection pin of the connector and the disconnected state is determined by a high logic state of the prescribed connection pin of the connector (col. 17, lines 47-50).

Regarding claim 11, Shetty discloses that a programmable logic device (PLD) senses the change of state and transfers the sensed information to the CPU (col. 17, lines 50-52).

Regarding claim 13, Shetty discloses that the PLD uses a pull-up resistor to determine a hardware protocol (col. 13, lines 51-54).

Regarding claim 14, Shetty discloses that transferring the sensing information to the internal CPU comprises: transmitting an interrupt request (IRQ) signal to the CPU when the change in the connection state of the connector is sensed (col. 17, lines 39-41; col. 6, lines 20-23; col. 17, lines 50-52);

sending an acknowledgement signal from the CPU (col. 17, line 17) and requesting that a hardware protocol mode value be transmitted to the CPU (col. 17, lines 39-41); and

transmitting a protocol connection mode value to the CPU (col. 17, lines 50-52).

Regarding claim 15, Shetty discloses that a programmable logic device sends the IRQ signal (col. 6, lines 20-23; col. 17, lines 50-52) and the protocol connection mode value to the CPU (col. 17, lines 50-52).

Regarding claim 16, Shetty discloses a method comprising:

sensing a connection and disconnection state of a connector configured to connect to a data circuit terminating equipment (DCE) by a programmable logic device (PLD) (col. 17, lines 39-41; col. 17, lines 50-52);

determining a "hardware protocol" communication convention(s) associated with the state or status of a hardware device when a state is changes (col. 17, lines 50-52);

sending an interrupt request signal to a CPU to inform the CPU of the change in the state of the connector (col. 6, lines 20-23; col. 17, lines 50-52);

sending a response to the interrupt request signal from the CPU to the PLD to request the PLD to send a hardware protocol mode value to the CPU (col. 6, lines 20-23; col. 17, lines 50-55);

transmitting the hardware protocol mode value from the PLD to the CPU (col. 17, lines 50-52); and

initializing parts of the router and normalizing a communication environment based on the stated information (col. 17, lines 60-61) and transmitted to the CPU (col. 17, lines 26-63).

Regarding claim 17, Shetty discloses that the hardware protocol is determined by at least one of the PLD and the CPU (col. 13, lines 51-54; col. 12, lines 63-65).

Regarding claim 19, Shetty discloses that the router is configured to automatically sense a change in hardware protocol without switching off the power to the router (col. 17, lines 39-41; col. 17, lines 50-52).

Regarding claim 20, including limitations discussed on claim 1, same rationale of rejection is applicable, further, Shetty discloses a data terminal equipment (DTE) device comprising:

a connector configured to provide a connection port to a data circuit terminating equipment (DCE) (fig. 2A, item 116; col. 3, lines 23-25);

a multi-protocol processor (fig. 2A, item 204) coupled to the connector and configured to transmit and receive two or more protocol signals through the connector (fig. 2A, item 110) and to initialize parts of the DTE after a connection of the connector to the DCE while power to the DTE is maintained (col. 8, lines 54-58); and

a CPU having a serial communication control function coupled to the multi-protocol processor to process data according to the communication environment of a connection network (fig. 2A, item 140).

Regarding claim 21, Shetty discloses that the multi-protocol processor comprises:

a multi-protocol transceiver to transmit and receive signals through the connector (fig. 2A, item 220A); and

a connection discrimination unit to initialize parts of the DTE based on the connection state of the connector (fig. 2A, item 202; col. 8, lines 54-58; col. 17, lines 39-41; col. 17, lines 60-61).

Regarding claim 22, Shetty discloses that the connection discrimination unit comprises:

a programmable logic device (PLD) (fig. 2A, item 204) coupled to receive connection state and hardware protocol information from the connector (col. 17, lines 39-41; col. 17, lines 50-51) and

transmit an interrupt request (IRQ) signal to the CPU in accordance with the state and protocol information (col. 17, lines 50-55).

Regarding claim 23, Shetty discloses that the PLD further transmits a protocol mode value (col. 17, lines 50-52) to the CPU after receiving an acknowledgement to the IRQ from the CPU (col. 17, lines 54-55).

Regarding claim 26, Shetty discloses that the PLD is coupled to the connector using a protocol mode line (col. 13, lines 51-54) and a state sensing line (col. 17, lines 39-41) (fig. 2A, item 110), and that the PLD is

coupled to the CPU using an IRQ signal line (col. 6, line 21), an ACK signal line (col. 17, line 17), and a data line (col. 6, line 26) (fig. 2A, item 1.4.6; col. 5, lines 65-67 - col. 6, lines 1-7).

Regarding claim 27, Shetty discloses at least one resistor coupled between the connector and the multi-protocol processor to sense at least one of a state of a cable between the connector and the multi-protocol processor and a protocol mode (col. 13, lines 51-54; col., 12, lines 63-65). Therefore, it would have been obvious to combine Yoshimura with Shetty for the benefit of detector simplicity.

6. Claims 5, 12, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shetty in view of Yoshimura (US 5,802,328).

Regarding claims 5 and 12, Shetty does not expressly disclose that the PLD uses a pull-up resistor to sense a connection and disconnection state of the connector;

however Yoshimura teaches that it is known that a pull-up resistor can be used to detect a state of connection or disconnection in a connector (col. 2, lines 57-60).

Shetty and Yoshimura are analogous art because they are both from the same field of endeavor of computer interface circuits. At the time of the invention it would have been obvious to a person of ordinary skill in the art to equip Shetty's connector with the ability to use a pull-up resistor to detect a state of connection and disconnection. The motivation for doing so would have been to provide a simple way to determine whether a card is inserted into the connector slot or not (col. 2, lines 61-62). Therefore, it would have been obvious to combine Yoshimura with Shetty for the benefit of detector simplicity.

Regarding claim 24, Shetty discloses that a first pull-up resistor is used to determine the hardware protocol information (col. 13, lines 51-54), however Shetty does not expressly disclose a second pull-up resistor that is used to determine the connection state.

Yoshimura teaches that it is known that a pull-up resistor can be used to detect a state of connection or disconnection in a connector (col. 2, lines 57-60).

Shetty and Yoshimura are analogous art because they are both from the same field of endeavor of computer interface circuits. At the time of the invention it would have been obvious to a person of ordinary skill in the art to equip Shetty's connector with the ability to use a pull-up resistor to detect a state of connection and disconnection. The motivation for doing so would have been to provide a simple way to determine whether a card is inserted into the connector slot or not (col. 2, lines 61-62). Therefore, it would have been obvious to combine Yoshimura with Shetty for the benefit of detector simplicity.

7. Claims 7, 18, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shetty in view of Ketelhut (US 4,764,868).

Regarding claims 7, 18 and 25, specifically, regarding claim 7, Shetty does not expressly disclose a transient voltage suppressor (TVS) coupled to absorb an electric shock generated upon connecting or disconnecting the connector with a corresponding receptacle; with respect to claim 18, Shetty does not expressly disclose absorbing an electrical shock generated during connection and disconnection of the router; and with respect to claim 25, Shetty does not expressly disclose that the connection discrimination unit further comprises a transient voltage suppressor, coupled to the connector to absorb an electrical shock generated upon connecting the connector during operation of the DTE.

Ketelhut discloses that it is known that a transient voltage suppressor can be used across the input port or connector of a device (fig. 7C, item 185, col. 12, lines 60-64).

Shetty and Ketelhut are analogous art because they are both from the same field of endeavor of input/output systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to connect a transient voltage suppressor in conjunction with Shetty's connector. The motivation for doing so would have been to prevent an unwanted electrical shock when inserting or removing Shetty's PCMCIA cards while the power is still on at the receiving device. Therefore, it would have been obvious to combine Ketelhut with Shetty for the benefit of preventing unwanted electrical shock.

Regarding claims 28-29, the PLD (202) is coupled to pins or holes of the connector (116), e.g. standard terminate pin fit ribbon cable conductor (Shetty column 5, lines 33-37)

Regarding claim 30, transferring to the CPU when the change in connection state is sensed (Shetty: column 5, lines 55-column 6, line 7, column 11, line 30 to column 12, line 8 and column 10, lines 65-column 11, line 29).

Regarding claim 31, interrupt service request is passed to the CPU when PLD sense a change in connection and disconnection state (column 17, line 39-52 and column 6, lines 20-23).

Response to arguments

8. Regarding claims 1-4, 8-11, 13-17, 19-23, 26 and 27 rejected under 35 U.S.C. 102(b) as being anticipated by Shetty it is argued that the applied prior art does not teach claim (1) limitation as recited. Specifically, does not teach "an apparatus for router configuration", because the desktop computer taught by Shetty is not a router, does not perform the features of a router.

In response to the above-mentioned argument, it is respectfully noted that, claim (1) does not recited any router functionalities argued. The recitation "for router configuration" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Rejection is sustained at least for this reason.

9. Regarding claims 1-4, 8-11, 13-17, 19-23, 26 and 27 rejected under 35 U.S.C. 102(b) as being anticipated by Shetty it is argued that the applied prior art does not teach claims (1 & 20) limitation as recited. Specifically, does not teach added limitation "a CPU having a serial communication control function coupled to the multi-protocol transceiver to process data from or for transmission to a communication network", because the Shetty's CPU (140) is coupled to a core logic (143) which in turn is coupled to a system bus (146), and further the CPU does not process data received from/to for transmission to a communication network.

In response to the above mentioned argument, it is noted that according to figure 2A, as noted by applicant, CPU (140) is coupled to a core logic (143) which in turn is coupled to a system bus (146) further coupled to ATA drivers (114 & 115) via standard cable 110, which are coupled to PCMCIA expansion board 218, coupled to multi-protocol transceiver 220A, which is coupled to connector (116). Further, CPU (140) is the heart of the computer system 101 and *controls the operations of the system*, and also the internal system memory 142. (column 1, lines 39-43). When communication is desired by a CPU with one of the peripherals coupled to the peripheral interface system (i.e. a pair of integrated circuits, referred to as a system adapter and a socket controller, see abstract), the peripheral interface system first determines which one of the multiple peripherals that are connected to it that the CPU desires to communicate with. The peripheral interface system then converts the signals from the system bus into the proper format for the required peripheral and controls the transmission of those signals to

the peripheral. Correspondingly, when a peripheral is *sending instructions or data to the CPU*, the peripheral comprising networked coupled devices (column 27, lines 5-25), the peripheral interface system converts the instructions or data from the peripheral into the format required by the CPU or controller and controls the transmission of those signals to the system bus (column 5, lines 55-column 6, line 7). For example, the system adapter 204 coupled to the system bus 146 for monitoring and controlling any communication which the CPU 140 is required to have with any of the peripherals, reading the address that appears on the system bus 146 used to access any of the peripherals that the host CPU desires to communicate with, then activates the peripheral and bi-directionally translates communication between therein (column 11, line 30 to column 12, line 8). Interrupts received from peripherals such as a service request are returned through the system bus 146 such that the host CPU can *process and respond* to the service request (column 10, lines 65-column 11, line 29). Arguments that a CPU does not process data to/from a communication network are not persuasive.

10. Regarding claims 1-4, 8-11, 13-17, 19-23, 26 and 27 rejected under 35 U.S.C. 102(b) as being anticipated by Shetty it is argued that the applied prior art does not teach claims (8 and 16) limitation as recited. Specifically, does not teach added limitation "sensing a change in a connection state of a connector between a router and a data circuit terminating equipment (DTE)", because the desktop taught by Shetty is not a router not element 101 performs routing functions.

In response to the above mentioned arguments, there are no routing functionalities noted in claim 8, applicant is entitled to be his/her own lexicographer, claim terminology is given the broadest reasonable interpretation in light of the specification (MPEP 2106 or 2111), in this claim term "router" is not defined in structure or functions in the claim nor is it further limited with any "routing" functionalities. For the purposes of examination it is a network related device. Claim limitation requires and/or recited the functions of sensing a change in a connection state of a connector (116) between device (101) and data circuit terminating equipment (122) (column 7, lines 39-41), the applied art meets claimed functionalities.

11. Regarding claims 1-4, 8-11, 13-17, 19-23, 26 and 27 rejected under 35 U.S.C. 102(b) as being anticipated by Shetty it is argued that the applied prior art does not teach claim (16) limitation as recited. Specifically, does not teach added limitation, sending an interrupt request signal to a CPU which response to the PLD.

In response to the above-mentioned argument, it is noted that Shetty teaches that the system adapter 204 recognizes interrupts received or service requests and will query the other peripherals which

will respond if they generated the interrupt, or service request. Once the type of service and what socket controller or associated peripheral has requested service is determined, the system adapter 202 (PLD) can then return the appropriate information to the system bus 146 such that the host CPU can process and respond to the service request (column 10, line 65 to column 11, line 29); When one of the peripherals is initiating a communication with the peripheral interface system, an interrupt signal request is sent to the system adapter integrated circuit. Each of the peripherals coupled to the peripheral interface system has a corresponding detection circuit for detecting when the peripheral interface system is communicating with that peripheral (column 6, lines 20-30). During a service request operation, the system adapter (202) provides a service request op code to have one of the socket controllers drive out on data lines what type of service request may be requested by one of the peripherals. The system adapter (202) upon receiving the type of service requests passes the service request type to the host CPU, the host CPU interrupts itself at an appropriate moment and goes out to perform the operations necessary to satisfy the type of service requested (column 17, lines 26-63).

12. Applicant's arguments filed 03/14/05 have been fully considered but not rendered persuasive.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prieto, B. whose telephone number is (571) 272-3902. The Examiner can normally be reached on Monday-Friday from 6:00 to 3:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, Andrew T. Caldwell can be reached at (571) 272-3868. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800/4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system, status information for published application may be obtained from either Private or Public PAIR, for unpublished application Private PAIR only (see http://pair-direct.uspto.gov or the Electronic Business Center at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

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PRIMARY EXAMINER

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TC 2100
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July 3, 2005